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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	10/665,164
Filing Date	9/18/2003
First Named Inventor	MELANSON
Art Unit	2817
Examiner Name	Unassigned
Attorney Docket Number	1437-CA

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US- 6,229,361	5/2001	Henwood	
	2	US- 6,690,240	02/10/2004	Maxim et al.	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	8/25/05

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Sheet 2 of 2

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	3	YOUNG et al., "A PLL Clock Generator with 5 to 110 MHz of Lock Range for Microprocessors," J. Solid-State Cir., 27(11):1599-1607, Nov. 1992	
	4	MANEATIS, J.G., "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques," J. Solid-State Cir., 31(11):1723-1732, Nov. 1996	
	5	MIJUSKOVIC et al., "Cell-Based Fully Integrated CMOS Frequency Synthesizers," J. Solid-State Cir., 29(3):271-279, Mar. 1994	
	6	NOVOF et al., "Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and ±50 ps Jitter," J. Solid-State Cir., 30(11):1259-1266, Nov. 1995	
	7	LEE and KIM, "A Low-Noise Fast-Lock Phase-Locked Loop with Adaptive Bandwidth Control," J. Solid-State Cir., 35(8):1137-1145, Aug. 2000	
	8	LIN et al., "A 1.4 GHz Differential Low-Noise CMOS Frequency Synthesizer Using a Wideband PLL Architecture," ISSCC Dig. Tech. Papers, San Francisco, CA, Feb. 2000, pp. 147-149	
	9	RHEE, W., "Design of High Performance CMOS Charge-Pumps in Phase Locked Loops," Proc. IEEE Int. Symp. Circuits and Systems, Orlando, FL, May 1999, pp. II.545-II.548	
	10	MAXIM et al., "A Low Jitter 125-1250 Mhz Process Independent 0.18µm CMOS PLL Based on a Sample-Reset Loop Filter," ISSCC Dig. Tech. Papers, San Francisco, CA, Feb. 2001, pp. 394-395	
	11	MAXIM and MAXIM, "A Novel Physical Model of Deep-Submicron CMOS Transistor Mismatch for Monte Carlo SPICE Simulation," Proc. IEEE Int. Symp. Circuits and Systems, Sidney, NSW, Australia, May 2001, pp. V.511-V.514	
	12	MAXIM et al., "Sample-reset Loop Filter Architecture for Process Independent and Ripple-Pole-Less Low Jitter CMOS Charge Pump PLL's," ISCAS 2001, 2001 IEEE Int. Symp., 4:766-769, May 6-9, 2001	

Examiner Signature		Date Considered	8/15/05

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